REMARKS/ARGUMENTS

Claims 1-7 and 11-21 are pending in this patent application.

A Preliminary Amendment was filed with this continuation application on September 26, 2003. Claims 1, 2 and 5 were previously amended in the Preliminary Amendment, and claims 8-10 were cancelled.

Claim Objections

In the Preliminary Amendment, claims 2 and 5 had been amended to overcome the Examiner's objections. Claim 10 has been cancelled.

Double Patenting

The Office Action stated:

> Claims 1-2, 4-6, and 11-21 of U.S. Patent No. 6,697,919 contains every element of claim 1-20 of the instant application and as such provisionally anticipates claim 1-20 of the instant application.

The chart presented in the office action did not reflect claim 1 as amended of this application nor claim 1 of granted 6,697,919 patent which has only 4 claims.

The action states this is an obviousness-type double patenting rejection. Particularly in view of the fact that the Preliminary Amendment does not appear to have been considered, a terminal disclaimer is premature at this stage of prosecution. Furthermore, it is respectfully submitted that the pending claims of the present Application and the issued claims of the granted U.S. Patent No. 6,697,919 are patentably distinct from each other. Should the Examiner believe that they are not patentably distinct from each other, a terminal disclaimer would be considered once the next Office Action indicates that all pending claims contain allowable subject matter.

35 U.S.C. 102(b) 1,2, 4-6, 16-18

Claims 1,2. 4-6 and 16-18 were rejected as anticipated by Computer Architecture: A Cumulative Approach by Patterson and Hennessy (herein referred to as "Patterson") under 35 U.S.C. § 102(b).

35 U.S.C. 103(a) 11 and 15

Claims 11 and 15 were rejected under 35 U.S.C. § 103(a) as obvious over the combination of Patterson and Safranek.

35 U.S.C. 103(a) 12-14

Claims 12-14 were rejected under 35 U.S.C. § 103(a) as obvious over Patterson in view of Laudon (U.S. Pat. No. 5,634,110).

Regarding the art rejections, claim 1 requires a protocol engine that implements a cache coherence protocol. The claimed protocol engine sends an initial invalidation request to no more than a first predefined number of nodes associated with bits that are set in an identification field of a directory entry. Applicants previously amended claim 1 to require that "the first predefined number of nodes being greater than one, but less than the number of nodes associated with set bits in the identification field." As such, the protocol engine sends at least two invalidation requests, but fewer invalidation requests than the number of nodes associated with the set bits in the identification field. A bit that is set in the identification field signifies that the memory line associated with that identification field is cached in at least one associated node.

The Examiner rejected claim 1 as anticipated by Patterson. Patterson generally discloses a bit vector in which each bit indicates whether a corresponding processor has a copy of a block of a particular data. See Patterson, page 680. However, Patterson discloses sending all processors identified in the bit vector as having a copy of the block invalidation messages. Patterson page 685 ("All processors in the set Sharers are sent invalidate messages...."). Thus, Patterson does not teach or suggest sending an initial invalidation request to more than one, but less than the number of nodes associated with set bits in an identification field.

Although the Examiner did not use Safranek or Laudon to reject claim 1, Applicants contend claim 1 is patentable over Safranek and Laudon. Safranek discloses several embodiments. In Figures 1A-1C and associated text at col. 9 lines 14-64, Safranek teaches a "head" node sending invalidation requests to all nodes needing to be invalidated. In Figures 7A-7C and associated text at col. 9

line 64-col. 10, line 36, Safranek also teaches the head node sending invalidation requests to all nodes needing to be invalidated, albeit with a degree of concurrency. In Figures 9A-9C and associated text at col. 11 line 64-col. 12, line 11, Safranek also teaches forwarding an invalidation request from one node to another node. In the embodiments of Figures 1A-1C and 7A-7C, the head node sends requests to all nodes, while in the embodiment of Figure 9, the head node only sends one invalidation request. As amended, claim 1 requires sending an initial invalidation request to more than one other node, but less than the number of nodes associated with set bits that indicate the nodes that have cached the associated memory line. Safranek, therefore, does not teach or suggest this feature of claim 1.

Laudon teaches fine and coarse bit vectors, but does not teach or suggest sending initial invalidation requests to a first predefined number of nodes "being greater than one, but less than the number of nodes associated with set bits in the identification field." Laudon, therefore, also does not teach or suggest all of the limitations of claim 1. Moreover, none of the cited art teaches or suggests the above-discussed feature of claim 1. For at least this reason, claim 1 is allowable. Claims 2-7 and 11-18 depend on or from claim 1 and thus are patentable for at least the same reason as claim 1.

35 U.S.C. 102(e) 19-21

Claims 19-21 were rejected as anticipated by Safranek (U.S. Pat. No. 6,493,809) under 35 U.S.C. § 102(b).

Independent claim 19 requires, among other limitations, input logic that receives a first invalidation request identifying a memory line and including a pattern of bits for identifying a subset of the nodes that potentially store cached copies of the memory line. Claim 19 also requires processing circuitry that sends a second invalidation request corresponding to the first invalidation request to a next node if the bits in the first invalidation request in fact identify the next node.

The Examiner rejected claim 19 as anticipated by Safranek. Safranek, however, does not appear to teach or even suggest including bits in the invalidation requests that identify nodes that potentially store cached memory

lines. By contrast, Safranek discloses the use of a "sharing list" that identifies the nodes that share a line of memory. Safranek does not disclose that the sharing list is transmitted as part of the invalidation requests. None of the other cited art satisfy the deficiency of Safranek. At least for this reason, claim 19 is allowable.

Claim 20 also requires input logic that receives a first invalidation request identifying a memory line and including a pattern of bits for identifying a subset of the nodes that potentially store cached copies of the memory line. Further, claim 20 comprises processing circuitry for determining a next node identified in the bits from the invalidation request. As explained above, Safranek does not appear to teach or suggest including bits in the invalidation requests that identify nodes that potentially store cached memory lines. The other art appears deficient as well. Claim 21 depends from claim 21 and thus is patentable for at least the same reason as claim 20.

Applicants respectfully request reconsideration and allowance of the pending claims. If any fees or time extensions are inadvertently omitted or if any fees have been overpaid, please appropriately charge or credit those fees to Hewlett-Packard Company Deposit Account Number 08-2025 and enter any time extension(s) necessary to prevent this case from being abandoned.

Applicants respectfully request that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

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